REMARKS

The non-final Office Action mailed July 31, 2002, has been received and reviewed. As of the May 22, 2002 Office Action, Claims 1-18 are pending in the application. Claims 1-18 presently stand rejected. Applicants have amended Claims 1-5, 8, 11-18. As of this amendment, Claims 1-18 are believed to be in condition for allowance and Applicants respectfully request reconsideration of the application as amended herein.

Objection to Title

The Examiner has required a new title, asserting that the original title of the invention is not descriptive. Applicant's have amended the title to read as follows: -- PORTABLE INEXPENSIVE RUGGED MEMORY, ASSEMBLY STRUCTURES AND METHODS OF FABRICATING SAME--.

35 U.S.C. § 112, ¶ 2 Indefiniteness Rejections

The Examiner has rejected Claims 1-11 and 13-18 under 35 U.S.C. § 112, ¶ 2 as being indefinite. Applicants have amended Claims 1-5, 11-13, 15, 17 and 18 to address errors in antecedent basis as noted by the Examiner and discovered by the Applicants. Applicants have also amended Claims 3, 4, 8, 11, 12, 17 and 18 to correct obvious errors in capitalization, punctuation and grammar. Additionally, Claim 17 has been amended to change claim dependency. Applicants believe Claims 1-11 and 13-18 are now definite and respectfully requests reconsideration of the Examiner's rejection of Claims 1-11 and 13-18 based on 35 U.S.C. § 112, ¶ 2 for indefiniteness.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,854,534 to Beilin et al.

Claims 1, 2, 4, 7-12 and 15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Beilin et al., U.S. Patent No. 5,854,534. Applicants have further amended Claims 1, 3-5 and 12-16 as explained more fully below. The standard for anticipation as set forth by the Court of Appeals for the Federal Circuit is as follows:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Regarding Claims 1, 3 and 4, Applicants have changed "memory materials" to --memory arrays-- throughout. Regarding Claims 1 and 3-5, Applicants have also changed "layer(s)" to --section(s)--. Regarding Claim 1 and deleted "layers of" as unnecessary and to further clarify the claimed invention. Regarding Claims 3-5 the language "of the" has also been deleted as being unnecessary and to further clarify the claimed invention.

Regarding Claims 12-14 and 16, Applicants have changed "materials" to --array-- or --arrays-- as appropriate. Regarding Claim 15, the language "or wires" (two occurrences) has been deleted to correct a potential ambiguity and to make Claim 15 more definite. Again, Beilin et al. fails to disclose "memory arrays" as recited in amended Claims 12-15.

Beilin et al. fails to disclose "memory arrays" as recited in amended Claims 1 and 12. As Claims 2, 4, 7-11 depend from amended Claim 1 and Claim 15 depends from amended Claim 12, Claims 2, 4, 7-11 and 15 are also believed to be allowable over Beilin et al. Applicants believe that Claims 1, 2, 4, 7-12 and 15 as amended are patentable over Beilin et al. and respectfully request reconsideration of the anticipation rejection based thereon.

35 U.S.C. § 103(a) Obviousness Rejections

The Examiner has rejected Claims 3, 5, 13, 14, 17 and 18 under 35 U.S.C. § 103(a) for obviousness. M.P.E.P. 706.02(j) sets forth the standard for a § 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). (Emphasis added).

<u>Obviousness Rejection Based on U.S. Patent No. 5,854,534 to Beilin et al. in view of U.S. Patent No. 5,185,689 to Maniar</u>

Claims 3, 5, 6, 13, 14 and 16-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Beilin et al. in view of Maniar. Applicants have amended Claims 1-5, 11-13 and 15-18 as explained above.

As neither Beilin et al. nor Maniar disclose "memory arrays", Claims 3, 5, 6, 13, 14 and 16-18 as amended are believed to be patentable over the asserted combination of Beilin et al. and Maniar. For these reasons, Applicants respectfully request reconsideration of the obviousness rejection of Claims 3, 5, 6, 13, 14 and 16-18 based on the asserted combination of Beilin et al. and Maniar.

Obviousness Rejection Based on U.S. Patent No. 5,854,534 to Beilin et al. in view of U.S. Patent No. 5,453,769 to Schantz et al.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Beilin et al. in view of Schantz et al. Applicant has amended Claim 1 as explained above. As Claim 6 depends from amended Claim 1, it also is believed to be nonobvious over the asserted combination of Beilin et al. and Schantz et al. Applicant respectfully requests reconsideration of the § 103(a) rejection of Claim 6.

Obviousness Rejection Based on U.S. Patent No. 5,854,534 to Beilin et al. in view of U.S. Patent No. 5,185,689 to Maniar further in view of U.S. Patent No. 4,623,986 to Chauvel

Claims 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Beilin et al. in view of Maniar and further in view of Chauvel. Applicant has amended Claim 16 as explained above. Claim 16 depends from amended Claim 12. For the above reasons, Claim 16 as amended is believed to be nonobvious over the asserted combination of Beilin et al. in view of Marniar and Chauvel. Applicant respectfully requests reconsideration of the § 103(a) rejection of Claim 16.

ENTRY OF AMENDMENTS

The amendments to Claims 1-5, 8, 11-18 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-18 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

The Commissioner is hereby authorized to charge any additional fee or to credit any overpayment in connection with this Amendment to Deposit Account No. 08-2025.

Respectfully Submitted,

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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend Claims 1-5, 8, 11-18 as follows:

1. (Amended) An assembly structure for a memory device, comprising:
a substrate having at least one fold line thereon, dividing the substrate into at least two sections;
a layer of memory [materials] arrays fabricated on each of the at least two sections, each [layer] section being disposed so that the [layers of] memory [materials] arrays on sections adjacent to each other form an interface in which the memory [materials] arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the fold line.

2. (Amended) The assembly structure recited in claim 1, wherein the fold line runs approximately down [the] a center of a definable portion of the substrate.

3. (Amended) The assembly structure recited in [C]claim 1, wherein at least one of the [layers] sections of memory [materials] arrays forming each [of the] interface[s] comprises semiconductor patterns.

4. (Amended) The assembly structure recited in [C]claim 1, wherein at least one of the [layers] sections of memory [materials] arrays forming each [of the] interface[s] comprises conductor line patterns.

5. (Amended) The assembly structure recited in claim 1, wherein the [layers] sections forming at least one [of the] interface[s] combine to provide a plurality of conductors and semiconductor patterns.

6. The assembly structure recited in claim 1, wherein the fold line comprises a series of aligned perforations.

7. The assembly structure recited in claim 1 wherein the fold line comprises at least one indentation in the substrate.

8. (Amended) The assembly structure recited in claim 1 wherein the fold line comprises at least one crease in the substrate.[.]

9. The assembly structure recited in claim 1, wherein the fold line comprises a change in a property of the substrate along the fold line.

10. The assembly structure recited in claim 1, wherein there are at least two fold lines on the substrate, providing at least three sections that fold over each other to produce at least two active memory devices.

11. (Amended) The assembly structure in [C]claim 10 wherein the three sections includes a center section having a set of conductor lines on both sides of the center section [substrate] to align with memory devices on both sides of the center section [substrate] after folding.

12. (Amended) An assembly structure for a memory device, comprising:
a common substrate having multiple sections;
a first layer of a memory [material] array disposed on a first section of the multiple sections[, of the memory device];
a second layer of a memory [material] array disposed on a second section of the multiple sections;
at least one fold line disposed on the common substrate to define alignment of the memory [materials] arrays on the first and second sections; and
wherein the sections may be folded on each other at the fold line to form an operable electronic device in the memory device.

13. (Amended) The assembly structure of claim 12 wherein the memory [materials] array on the first section comprise a first plurality of conductor lines and the memory [materials] array on the second section comprise a second plurality of conductor lines, and wherein at least one of the memory [materials] arrays comprise semiconductor materials.

14. (Amended) The assembly structure of claim 13 wherein the memory [materials] arrays of the first and second sections are fabricated so that, with the first and second sections folded on each other at the fold line, the first and second pluralities of conductor lines and the

semiconductor materials are aligned with each other to form the operable electronic device in the memory device.

15. (Amended) The assembly structure recited in claim 13, wherein the first plurality of [conductors] conductor lines are formed with an array of parallel conductors [or wires] spaced across the first section, and the second plurality of [conductors section] conductor lines are formed with an array of parallel conductors [or wires] spaced across the second section, the plurality of [conductors] conductor lines on the second section being perpendicular to the plurality of [conductors] conductor lines on the first section.

16. (Amended) The assembly structure recited in claim 13 wherein the first and second sections are folded along the fold line so that the layers of memory [material] arrays are in contact with each other, and wherein at least one of the first and second sections has semiconductor materials and patterns thereon to form a matrix of memory cells.

17. (Amended) The assembly structure recited in [C]claim [13] 16 wherein the first plurality of [conductors of the first section] conductor lines are fabricated with first narrowing cross-section areas at points where the memory cells are capable of a permanent change of state.

18. (Amended) The assembly structure recited in [C]claim 17, wherein the second plurality of [conductors in the second section] conductor lines includes second narrowing cross-section areas configured to align with the first narrowing cross-section areas [of the first section].